AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A plasma display panel, comprising:

a first substrate;

a second substrate facing the first substrate ~~with a discharge space therebetween~~;

a plurality of address electrodes on the second substrate, the address electrodes extending in a first direction;

a plurality of other electrodes on the first substrate, the other electrodes extending in a second direction different than the first direction;

a plurality of barrier ribs on the second substrate to form a plurality of discharge cells, the plurality of barrier ribs extending in the first direction;

a sealing layer located between the first substrate and the second substrate, the sealing layer extending in the second direction, wherein the sealing layer has a thermal expansion coefficient of approximately $65x10^{-7}$~$80x10^{-7}$/°C;

at least one of a buffer layer or a dielectric layer formed between the first substrate and the sealing layer, wherein the at least one of the buffer layer or the dielectric layer has the following composition: PbO at a ratio of 45% to 55%, B_2O_3 at a ratio of 10% to 20% and SiO_2 at a ratio of 15%-25%; and

a protective film formed on the at least one of the buffer layer or the dielectric layer, wherein the at least one of the buffer layer or the dielectric layer has a thermal expansion coefficient different from the thermal expansion coefficient of the sealing layer.

2. (Canceled)

3. (Previously Presented) The plasma display panel according to claim 1, wherein the buffer layer has the thermal expansion coefficient different from a thermal expansion coefficient of the first substrate.

4-6. (Canceled)

7. (Previously Presented) The plasma display panel according to claim 1, wherein the first substrate has a thermal expansion coefficient of approximately $80X10^{-7}$~$95X10^{-7}$/°C.

8. (Canceled)

9. (Previously Presented) The plasma display panel according to claim 1, wherein the buffer layer has the thermal expansion coefficient of approximately $72X10^{-7}$~$86X10^{-7}$/°C.

10. (Canceled)

11. (Previously Presented) The plasma display panel according to claim 1, wherein the plasma display panel includes both the buffer layer and the dielectric layer such that the buffer layer is provided between the first substrate and the dielectric layer and such that the dielectric layer is provided between the buffer layer and the protective film.

12. (Previously Presented) The plasma display panel according to claim 11, wherein the buffer layer is formed to extend from the dielectric layer.

13. (Previously Presented) The plasma display panel according to claim 11, wherein the buffer layer is separately formed of a different material than the dielectric layer.

14-25. (Canceled)

26. (Currently Amended) A plasma display panel, comprising:

a first substrate;

a second substrate arranged with respect to the first substrate ~~such that a discharge space is provided therebetween~~;

a plurality of address electrodes on the second substrate, the address electrodes extending in a first direction;

a plurality of other electrodes on the first substrate, the other electrodes extending in a second direction, the second direction being different than the first direction;

a plurality of barrier ribs on the second substrate, the plurality of barrier ribs extending in the first direction;

a sealing layer between the first substrate and the second substrate, the sealing layer provided along the second direction, wherein the sealing layer has a thermal expansion coefficient of approximately $65x10^{-7}$~$80x10^{-7}$/°C; and

at least one of a buffer layer or a dielectric layer formed between the first substrate and the sealing layer, wherein the at least one of the buffer layer or the dielectric layer has a thermal expansion coefficient of approximately $72x10^{-7}$/°C to $85x10^{-7}$/°C, and wherein the thermal expansion coefficient of the at least one of the buffer layer or the dielectric layer is different from the thermal expansion coefficient of the sealing layer.

27. (Currently Amended) The plasma display according to claim 26, wherein the sealing layer ~~extends~~ is provided in a ~~longitudinal~~ third direction from a first end to a second end, the first end located proximal to the first substrate and the second end located proximal to the second substrate, the buffer layer provided only in the area between the first end of the sealing layer and the first substrate.

28. (Previously Presented) The plasma display according to claim 26, further comprising:

another sealing layer between the first substrate and the second substrate; and

another buffer layer formed between the first substrate and the another sealing layer, the another buffer layer to compensate thermal stress of the first substrate and the another sealing layer.

29. (Previously Presented) The plasma display panel according to claim 28, wherein the at least one of the buffer layer or the dielectric layer is the buffer layer, and the plasma display panel further comprises:

an upper dielectric layer formed on the first substrate between the buffer layer and the another buffer layer; and

a protective film formed on the upper dielectric layer.

30. (Previously Presented) The plasma display panel according to claim 26, wherein the thermal expansion coefficient of the buffer layer is different from a thermal expansion coefficient of the first substrate.

31-38. (Canceled)

39. (Previously Presented) The plasma display panel according to claim 26, wherein the at least one of the buffer layer or the dielectric layer has the following composition: PbO at a ratio of 45% to 55%, B_2O_3 at a ratio of 10% to 20% and SiO_2 at a ratio of 15% to 25%.

40-43. (Canceled)

44. (Previously Presented) The plasma display panel according to claim 1, wherein the at least one of the buffer layer of the dielectric layer has a thickness greater than 35 μm and less than 39 μm between the sealing layer and the first substrate.

45. (Previously Presented) The plasma display panel according to claim 26, wherein the at least one of the buffer layer of the dielectric layer has a thickness greater than 35 μm and less than 39 μm between the sealing layer and the first substrate.

46. (New) The plasma display panel according to claim 27, wherein a distance from the second end of the sealing layer to the first end of the sealing layer in the third direction is greater than a height of each of the plurality of barrier ribs.

47. (New) The plasma display panel according to claim 26, wherein the sealing layer is provided from the second substrate toward the first substrate to a height greater than a height of each of the plurality of barrier ribs.

48. (New) The plasma display panel according to claim 26, further comprising a phosphor formed on the plurality of barrier ribs, wherein the sealing layer is provided from the second substrate to a height that is greater than a height of the phosphor on the barrier ribs.

49. (New) The plasma display panel according to claim 26, wherein the sealing layer comprises glass powder, solvent and binder.

50. (New) The plasma display panel according to claim 1, wherein the sealing layer is provided from the second substrate toward the first substrate to a height greater than a height of each of the plurality of barrier ribs.

51. (New) The plasma display panel according to claim 1, further comprising a phosphor formed on the plurality of barrier ribs, wherein the sealing layer is provided from the second substrate to the height that is greater than a height of the phosphor on the barrier ribs.

52. (New) The plasma display panel according to claim 51, wherein the sealing layer comprises glass powder, solvent and binder.